

1 HIGH-SPEED OPTICAL DATA LINKS

2
3 CROSS-REFERENCE TO RELATED APPLICATION

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5 This application claims the benefit of U.S. Provisional
6 Application serial no. 60/306,697, filed 20 July 2001.

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8 Field of the Invention

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10 This invention relates to optical transmitters,
11 receivers, and transceivers.

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13 More specifically, this invention relates to data links
14 in optical transmitters, receivers, and transceivers.

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16
17 Background of the Invention

18
19 Optical transmitters, receivers and transceivers are
20 used for converting electrical data into optical data for
21 transmission on optical fibers and for converting optical
22 data back into electrical data for processing by network
23 equipment. Normally, an optical transmitter includes a
24 light source, such as a laser driver and a laser diode, and

1 an optical receiver includes a light conversion device,
2 such as a post amplifier, a trans-impedance amplifier and a
3 PIN photodiode or an APD. The transmitter or receiver is
4 generally mounted on a network circuit board to interface
5 with other data processing IC chips, such as a serializer
6 or de-serializer, a data framer for coding, such as 8B/10B
7 coding, and a higher level data control IC. This type of
8 structure, however, fails to perform when the data
9 transport rate reaches around 10 Gbps or beyond, as the
10 electric traces on the printed circuit board introduce
11 noises and jitters and distort the signal integrity at such
12 a high frequency.

13

14 Current technology requires that a serializer and de-
15 serializer be integrated into the transmitter and receiver
16 module or modules to allow electrical interfaces to operate
17 at lower frequency. As an example, for an OC192 data rate,
18 the electrical interfaces for the data link module will
19 require 16 channels of 622 Mbps. The module, which is
20 called a fiber optical transponder, can then be mounted
21 onto the board to interface with other IC chips to fulfill
22 the network management function. Consequently, the module
23 requires many electrical interfaces, typically with more
24 than 50 pins. The large number of pins and the extra

1 internal circuitry dictates that the module size is large.

2 The power consumption is also a serious issue.

3

4 It would be highly advantageous, therefore, to remedy
5 the foregoing and other deficiencies inherent in the prior
6 art.

7

8 Accordingly, it is an object the present invention to
9 provide a new and improved high-speed optical data link.

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11 Another object of the present invention is to provide a
12 new and improved high-speed optical data link capable of
13 conveying data at around 10 Gbps rates or beyond.

14

15 And another object of the present invention is to
16 provide a new and improved high-speed optical data link
17 that is simple and relatively inexpensive to manufacture.

18

19 Still another object of the present invention is to
20 provide a new and improved high-speed optical data link
21 that is smaller than prior art devices and less electrical
22 pin counts capable of conveying information at similar
23 rates.

1 Summary of the Invention

2

3 Briefly, to achieve the desired objects of the present

4 invention in accordance with a preferred embodiment

5 thereof, provided is a high-speed optical data link

6 including a system board with first and second ASICs

7 mounted thereon. The first ASIC includes a clocking and an

8 equalization function for recovering distorted data. The

9 second ASIC is electrically coupled to the first ASIC for

10 conveying electrical signals therebetween and the second

11 ASIC includes one of a clocking and an equalization

12 function for recovering distorted data.

13

14 In a more specific embodiment, a high-speed optical

15 data link includes a first ASIC coupled to convey

16 electrical information to a remote circuit and a second

17 ASIC electrically coupled to the first ASIC for conveying

18 electrical signals therebetween. A fiber optic receiver

19 module is mounted on the system circuit board and includes

20 a photo diode positioned to receive optical signals from a

21 remote source, a trans-impedance amplifier electrically

22 coupled to the photo diode, and a post-amplifier, such as a

23 limiting amplifier or an auto-gain control circuitry,

24 electrically coupled to the trans-impedance amplifier and

1 to the second ASIC. The second ASIC includes a clocking
2 and an equalization function for data integrity and the
3 first ASIC includes a function for recovering distorted
4 data through the same clocking and an equalization scheme
5 as provided by the second ASIC.

6

7 In another more specific embodiment a high-speed
8 optical data link also includes a first ASIC coupled to
9 receive electrical information from a remote circuit and a
10 second ASIC electrically coupled to the first ASIC for
11 conveying electrical signals therebetween. A fiber optic
12 transmitter module mounted on the system circuit board
13 includes a laser positioned to convey optical signals to a
14 remote source and a laser driver electrically coupled to
15 the laser and to the second ASIC. The first ASIC includes
16 a clocking and may include an equalization function for
17 data transmission and the second ASIC includes an
18 equalization function for recovering distorted data through
19 the same clocking. It should be noted that both of the
20 last two embodiments described can, optionally, be packaged
21 and included on a common board with the first and second
22 ASICs being common.

23

24 The embodiments described above include a novel method

1 of electrically communicating information at 10-gigabits
2 per second or beyond on a circuit board. The method
3 includes the steps of providing a system circuit board
4 including a first position and a second position, receiving
5 electrical signals from an external source at the first
6 position on the system circuit board, clocking and
7 equalizing the electrical signals on the system circuit
8 board for providing signals with integrity, conveying the
9 equalized signals to the second position on the system
10 circuit board, and receiving the equalized signals at the
11 second position and recovering distorted signals using a
12 de-clocking and re-timing step.

1 Brief Description of the Drawings

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3 The foregoing and further and more specific objects and

4 advantages of the invention will become readily apparent to

5 those skilled in the art from the following detailed

6 description of a preferred embodiment thereof, taken in

7 conjunction with the drawings in which:

8

9 FIG. 1 is a simplified block diagram/top plan of a

10 prior art optical data link; and

11

12 FIG. 2 is a simplified high speed optical data link in

13 accordance with the present invention.

Detailed Description of the Drawings

Referring to FIG. 1, a simplified block diagram/top plan of a prior art optical data link 100 is illustrated. Data link 100 includes a system board 101 with a fiber optic transponder 110 mounted thereon. Electrical connections for the various components of transponder 110 are not illustrated since they are provided, in a well-known manner, through internal connections in the mounting structure. Transponder 110 includes a serializer/deserializer 112 electrically connected to a transimpedance amplifier and post-amplifier 114, which is in turn electrically connected to PIN photodiode 116. Photodiode 116 is positioned to receive modulated light signals from an optical fiber, represented by an arrow 140. Serializer/deserializer 112 is also electrically connected to a laser driver 118, which is in turn connected to drive a laser diode 120. Laser diode 120 is positioned to supply modulated output light to an optical fiber, represented by an arrow 130. Input and output electrical signals for transponder 110 are supplied by an electric interface, including connectors and printed circuit board copper traces designated 160, from board level IC chips, generally designated 150.

1 The connectors and traces of electrical interface 160
2 on printed circuit board 101 introduce noises and jitters
3 that distort the signal integrity, at high frequencies
4 (e.g., in the 10-gigabits per second range or above), of
5 signals communicated between transponder 110 and board
6 level IC chips 150. Because of this distortion, electrical
7 interface 160 must operate at lower frequencies, which
8 requires a large number of channels. For example, a 10
9 Gbps signal is converted by serializer/deserializer 112
10 into 16 channels of differential signals 622 Mbps.
11 However, the use of serializer/deserializer 112 in
12 transponder 110 and the 16 channels, greatly increases the
13 number of pins or connections in electrical interface 160.
14 The 16 channels and associated connections greatly
15 increases the size and power requirements of transponder
16 110.

17
18 Turning now to FIG. 2, a simplified high-speed optical
19 data link 200 in accordance with the present invention is
20 illustrated. Data link 200 includes a system board 201
21 with a fiber optic transceiver 210 mounted thereon.
22 Electrical connections for the various components of
23 transceiver 210 are not illustrated since they are
24 provided, in a well-known manner, through internal

1 connections in the mounting structure. Transceiver 210
2 includes a first ASIC 212 electrically connected to a light
3 converting device, illustrated herein for exemplary
4 purposes as a transimpedance/post amplifier 214
5 electrically connected to a PIN photodiode 216. Photodiode
6 216 is positioned to receive modulated light signals from
7 an optical fiber, represented by an arrow 240. ASIC 212 is
8 also electrically connected to a light generating device,
9 herein illustrated for exemplary purposes only as a laser
10 driver 218 connected to drive a laser diode 220. Laser
11 diode 220 is positioned to supply modulated output light to
12 an optical fiber, represented by an arrow 230.

13

14 Input and output electrical signals for transceiver 210
15 are supplied by an electric interface, including connectors
16 and printed circuit board copper traces and the like
17 designated 260. Board level IC chips, generally designated
18 250, include a second ASIC 252, which is connected by
19 electrical interface 260 to first ASIC 212 in transceiver
20 210. While a transceiver incorporating both an optical
21 transmitter and an optical receiver is illustrated in this
22 example for purposes of explanation, it will be understood
23 that the pair of ASICs can be used with single optical

1 transmitters, single optical receivers, optical
2 transceivers, or any combination of these devices.

3

4 By incorporating the pair of ASICs in the optical
5 transmitter, receiver, or transceiver, a 10 Gbps or higher
6 serial electrical interface can be established directly
7 between transceiver 210 and system board 250 through normal
8 electrical interfaces 260, such as pin-grid-array, ball-
9 grid-array, edge connectors, etc. A clock data recovery
10 (CDR) is built into each of the ASICs 212 and 252. Also,
11 each of the ASICs 212 and 252 operate to receive electrical
12 signals from interface 260 and to transmit electrical
13 signals through interface 260. Either ASIC 212 or ASIC 252
14 retimes and clocks the signal and provides driving power
15 for the transmitting portion. For the receiving portion of
16 ASICs 212 and 252, they both handle and recover the
17 distorted data due to high frequency signal transmitting
18 directly on the electric traces of the circuit board.

19

20 The clock and equalization/retiming can be performed
21 using a variety of techniques, one of which is described in
22 detail in a paper by Abhijit Phanse presented to the IEEE
23 in New Orleans in September 2000, a copy of which is
24 appended hereto and incorporated by reference.

1 Thus, each fiber optic data link includes a fiber optic
2 transmitter module with a first ASIC to equalize/retime and
3 recover electric data distorted by the electric traces on
4 the system board and a second ASIC mounted in the system
5 printed circuit board to clock and equalize the electric
6 data and provide driving power for transmitting to the
7 optical transmitter module through electric traces on the
8 printed circuit board. The described fiber optic data link
9 system operates at a data rate of more than 5 Gbps. In a
10 preferred embodiment, the second ASIC on the system board
11 includes a clocking and equalization function for data
12 transmission over printed circuit traces and the first ASIC
13 in the transmitter module includes a function for
14 recovering the distorted data through the same coding and
15 clocking scheme provided by the second ASIC. In another
16 embodiment, the second ASIC on the system board includes a
17 serializer for data serialization, a clocking, and an
18 equalization function, and the driving power for data
19 transmission over printed circuit traces, and the first
20 ASIC in the transmitter module includes a function for
21 recovering the distorted data through the same clocking
22 scheme provided by the second ASIC.

1 As a typical example, the fiber optic data link
2 includes a fiber optic receiver module mounted on a system
3 printed circuit board. The fiber optic receiver module
4 includes a photo diode, a trans-impedance amplifier, a
5 post-amplifier, and a first ASIC to clock and equalize
6 electric data and provide electric driving power for
7 transmitting to the system printed circuit board through
8 electrical traces on the printed circuit board. The system
9 printed circuit board includes a second ASIC connected and
10 designed to recover electric data distorted by the electric
11 traces on the system printed circuit board. In this
12 embodiment, the first ASIC on the receiver module includes
13 a clocking and retiming function for data transmission and
14 provides electric signal driving power, and the second ASIC
15 on the system board includes a function for recovering the
16 distorted data through the same clocking scheme provided by
17 the first ASIC. Also in this example, the first ASIC on
18 the receiver module includes a clocking and equalization
19 function for data transmission, and the second ASIC on the
20 system board includes a function for recovering the
21 distorted data through the same clocking scheme provided by
22 the said first ASIC and may further include a de-serializer
23 for data de-serialization.

1 In yet another example, a fiber optic data link system
2 includes a fiber optic transceiver module mounted on a
3 system printed circuit board, the fiber optic transceiver
4 module includes a transmitter, including a laser diode and
5 a laser driver, a receiver and a first ASIC.

6
7 The receiver includes a photo diode, a trans-impedance
8 amplifier and a post-amplifier. The first ASIC performs
9 clocking and equalization/retiming functions to the data
10 coming from the receiver and provides driving power for
11 transmitting to the system board through electric traces on
12 the printed circuit board. The first ASIC also performs
13 the function of recovering distorted electric data coming
14 from the system board through the electric traces on the
15 printed circuit board for transmitting to the transmitter.
16 The system printed circuit board includes a second ASIC for
17 recovering electric data coming from the optical
18 transceiver and distorted by the electric traces on the
19 system printed circuit board and clocking and equalizing
20 the electric data and providing driving power for
21 transmission on the printed circuit board to the optical
22 transceiver module.

1 The first ASIC on the transceiver module also includes
2 a clocking and equalization/retiming function for data
3 transmission on the receiver side, a function for
4 recovering the distorted data through the same clocking
5 scheme as provided by the second ASIC on the system board,
6 and the second ASIC on the system board includes a function
7 for recovering the distorted data through the same clocking
8 scheme provided by the first ASIC and clocking functions
9 for transmitting data to the transceiver through the
10 electric traces on the circuit board. The first ASIC on
11 the transceiver module also includes a clocking function
12 and coding function for data equalization on the receiver
13 side, a function for recovering the distorted data through
14 the same coding scheme as provided by the second ASIC on
15 the system board.

16

17 The second ASIC on the system board includes a function
18 for recovering the distorted data through the same retiming
19 and clocking scheme provided by the first ASIC, a clocking
20 and equalization function for transmitting data to the
21 transceiver through the electric traces on the circuit
22 board, a serializer function for data serialization and de-
23 serializer for data de-serialization.

1 Thus, a new and improved high speed optical data link
2 is disclosed which includes a pair of ASICs that provide
3 clocking and equalization functions for transmitting data
4 through system boards at rates in the 10-Gbps range or
5 above. By doing so, the fiber optic module, such as
6 transmitter, receiver or transceiver, will have smaller
7 size, lower power consumption, and less electrical pin
8 counts. It is also easier to make the transceiver
9 pluggable.

10

11 Various changes and modifications to the embodiments
12 herein chosen for purposes of illustration will readily
13 occur to those skilled in the art. To the extent that such
14 modifications and variations do not depart from the spirit
15 of the invention, they are intended to be included within
16 the scope thereof, which is assessed only by a fair
17 interpretation of the following claims.

18

19 Having fully described the invention in such clear and
20 concise terms as to enable those skilled in the art to
21 understand and practice the same, the invention claimed is: